Notice of Allowability	Application No.	Applicant(s)	
	10/687,980	MORAVEJI, FARHOOD	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *original filing (Oct 16, 2003) and Interview (Dec 9, 2004)*.

2. ☒ The allowed claim(s) is/are *1-28*.

3. ☒ The drawings filed on *16 October 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12092004* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicant's representative Patrick T. Bever (Reg. No. 33,834) on Dec 9, 2004.

The application has been amended as follows:

Page 6, line 3 of paragraph 0024: changed "CS2" to --CS3--;

line 2 of paragraph 0025: changed "300" to --200--;

Page 7, line 1: changed second occurrence of "211" to --212--;

Page 9, line 3 of paragraph 0032: changed "S1" to --S1)--;

Page 12, line 3 of paragraph 0044: deleted "and";

Claim 10, line 7: changed "first" to --second--;

Claim 26, lines 4-5: changed "constant-on third switch" to --third constant-on switch--; and

Claim 27, line 5: changed "constant-on third switch" to --third constant-on switch--.

Most of the changes made to the disclosure and claims address/correct inadvertent oversights. The two changes made on page 6 ensure the reference designators accurately correspond to those shown in Fig. 2A. Page 7 now clearly identifies the two different capacitors shown in Fig. 2B. Page 9 had a missing closing parenthesis added, and an unnecessary term was deleted from page 12. Claim 10 was amended to distinguish the control branches, and their

respective current sources and controllable switches. [One of ordinary skill in the art would understand claim 10, lines 2-6, "first control branch" correspond to one control branch (e.g. see B(C1) of Fig. 2A), wherein the originally recited "first control branch" of line 7 actually corresponds to another (i.e. second) "control branch") (e.g. see B(C2) of Fig. 2A). Claims 26-27 were both changed to provide consistent labeling with respect to the first-seventh constant-on switches.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses a differential charge pump, or related method, as recited within independent claims 1, 12, and 18. More specifically, none of the references clearly shows or discloses a common mode voltage at the first/second plates of a capacitive structure/charging capacitor when first/second signals are at the same level as recited within claims 1 and 12, upon which respective claims 2-11, and 13-17 depend. Also, none of the references shows/discloses the first-third transistors as recited within claim 18, wherein the first/second transistors are coupled to the first/second plates, respectively of the capacitive structure, and a voltage control circuit regulates the gate of the third transistor (which is also coupled to the gates of the first and second transistors). Claims 19-28 depend on claim 18. Since there is no motivation to modify or combine any prior art reference(s) to ensure any of the above specific limitations are met, the claims are deemed patentably distinct over the prior art of record.

Claims 1-28 are allowed.

PRIOR ART

The prior art references on the accompanying PTO-892 are cited for interest and documentation purposes only. Of special interest is the Japanese patent, wherein Fig. 7 shows first control branch 11,SW1,SW2,12; second control branch 13,SW3,SW4,14; and capacitive structure C1 having first/second plates coupled between the control branches at Vout1/Vout2, respectively. Each control branch charges and discharges a corresponding plate of C1. For example, current source 11 and switch SW1 allow the first plate to charge when first signal UP closes switch SW1, wherein switch SW2 and current source 12 discharge the first plate when second signal DN closes switch SW2. Switch RS1 allows a common mode type voltage (e.g. the same voltage) to be applied to both plates when it is closed. However, switch RS1 is controlled by a reset signal during initialization operations. Fig. 6 of the Bruccoleri et al. reference is also of special interest. When signals UP and DOWN are both equal to 0, current sources Gc1 and Gc4 are both on, allowing current I flowing from each of current sources Gb1 and Gb2 to flow past the filter network (e.g. C1,R1,C2), and no current to flow through the filter network. In this circuit, Gb1 and Gb2 would be at least part of the control branches for charging and discharging the first/second plates of the capacitive structure, and therefore would not be considered separate common mode branches for charging/discharging the plates to a common mode voltage. Also, since Gc1-Gc4 are each controlled by a separate signal, the reference does not clearly indicate a common mode voltage is on the first/second plates when the first/second signals are at the same level. For example, if the voltages at nodes A and B are different, and if UP = DOWN = 0, no current flows through the filter network. Therefore, the different voltages on nodes A and B will be maintained (e.g. see column 3, line 58 – column 4, line 1), and the plates will not share a

common mode voltage. Eschauzier shows a differential charge pump type circuit in Fig. 5 with a capacitive structure Ci that has its plates charged and discharged in accordance to signals applied to the gates of M1 and M2 (e.g. see IN+ and IN- of Figs. 2 and 4). Although the circuit has common mode control, the common mode voltage Vcm is applied to the bases of transistors Q3, and Q6-Q7, and not to both plates of Ci. Also, since the input signals are apparently complementary to one another, the only time they will be equal will be when they transition (i.e. when the rising and falling edges of the two signals temporarily cross each other). If current sources I1/I2 are replaced with first/second transistors coupled to the first/second plates, respectively of capacitive structure Ci, there is still no motivation to add a third transistor with its gate coupled to the gates of the first/second transistors, wherein the gate voltage is regulated by a voltage control circuit (e.g. as recited within claim 18).

A copy of the Japanese patent is being submitted to the applicant. The other references are U.S. Patents, and are readily available for review and consideration.

There is no motivation to modify any of the prior art references reviewed and considered to ensure the first/second plates are coupled to a common mode voltage when the first/second signals are at the same level, or the first/second plates are associated with the first-third transistors, as recited within at least one of the present application's independent claims.

Any comments considered necessary by the applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

9 December 2004